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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/703,144	10/31/2000	David Hoyle	Ti-30564	1032

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EXAMINER	
O BRIEN, BARRY J	

ART UNIT	PAPER NUMBER
2183	7

DATE MAILED: 03/24/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/703,144	HOYLE ET AL.
	Examiner	Art Unit
	Barry J. O'Brien	2183

-- Th MAILING DATE of this communication appears on the cov r sheet with the correspondenc address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 January 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4,10-13 and 15-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-2, 4 and 15-19* is/are allowed.

6)☒ Claim(s) *10-13 and 20-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☒ Interview Summary (PTO-413) Paper No(s)/Mail Date. 7.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-2, 4, 10-13 and 15-24 have been examined.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed on record in the file: Extension of Time as received on 1/14/2004 and Amendment A as received on 1/14/2004.

Specification

3. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

4. The applicant is requested to review the specification and update the status of all co-pending applications made mention of, replacing attorney docket numbers with current U.S. application or patent numbers when appropriate.

Claim Objections

5. Claims 4, 12 and 20 are objected to because of the following informalities:

   a. Claim 4 recites the limitation "The digital system of claim 3" on its first line. There is lack of antecedent basis for claim 3, as it was canceled by the present amendment. Please correct the claim language to read, "The digital system of claim 1" in order to provide correct antecedent basis.

b. Claim 12 is present in the listing of claims on p.8-13 of the present amendment. However, it is not listed as one of the pending claims, as one of the claims that has been cancelled on p.14 of the present amendment, or in the remarks section. The examiner believes that claim 12 was meant to be cancelled, as it encompasses the same scope as cancelled claim 3. Please correct this problem by either canceling claim 12, or properly addressing the claim.

c. Claim 20 recites the limitation "further comprising the step of" on its first and second lines. However, the claim consists of multiple steps. Please correct the claim language to read, "further comprising the steps of".

Appropriate correction is required.

Response to Arguments

6. Applicant's arguments, see Amendment A, filed 1/14/2004, with respect to the rejection(s)of claim(s) 1-14 under Black et al. have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection for claims 10-13 and 20-24 is made in view of the *Intel Pentium Processor Family Developer's Manual Vol.3: Architecture and Programming Manual.*

Claim Rejections - 35 USC § 112

7. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

8. Claim 23 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 23 recites the limitation "said predetermined address boundary" in line 5 of the claim. There is insufficient antecedent basis for this limitation in the claim. For the purposes of the examination, the examiner will assume that claim 23 simply adds a displacement value to the program counter when executing a branch-decrement instruction that was fetched in a fetch packet.

Claim Rejections - 35 USC § 102

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

10. Claims 10, 12-13 and 20 are rejected under 35 U.S.C. 102(b) as being anticipated by the *Intel Pentium Processor Family Developer's Manual Vol.3: Architecture and Programming Manual.*

11. Regarding claim 10, the *Pentium Processor Family Developer's Manual* has taught a method of operating a digital system having a microprocessor with a conditional branch-decrement instruction, comprising the steps of:

a. Fetching a conditional branch-decrement instruction for execution (see p.3-10 and Sec.3.5.3.1 on p.3-20). Here, the REP instruction (see p.25-266) is a conditional

branch-decrement instruction whose operation includes conditional branching and a decrement of a counter register (see p.25-267).

b. Testing a test register selected by the conditional branch-decrement instruction to determine if the contents of the test register meet a first condition (see "While CountReg<>0" on p.25-267). Here, the test register is CX/ECX which is selected by the REP instruction. Although the REP instruction cannot specify a different register, it is still selecting the CX or ECX register to be used as the test register.

c. Providing a branch address to a program counter to cause a branch if the contents of the test register meet the first condition (see p.25-267). Here, both the servicing of pending interrupts, the performance of a primitive string instruction, and the IF-THEN-ELSE constructs will be branching, and inherently cause the PC to change as every instruction that is executed has a new PC address. This branching will only occur if the test register has met the first condition, as in order to get into the while loop the test register had to have met the first condition (see p.25-267).

d. Modifying the contents of the test register if the contents of the test register meet the first condition (see "CountReg ← CountReg –1" on p.25-267). Here, the test register has met the first condition (see "While CountReg<>0" on p.25-267), and therefore is modifying the test register if the first condition has been met.

12. Regarding claim 12, the *Pentium Processor Family Developer's Manual* has taught the method of claim 10, wherein the step of modifying decrements the test register (see "CountReg ← CountReg –1" on p.25-267).

13. Regarding claim 13, the *Pentium Processor Family Developer's Manual* has taught the method of claim 10, wherein the steps of testing, providing, and modifying are all performed during a same execution phase of the microprocessor (see p.25-268). Here, the checking of the count register (step 2), the interrupt processing and string operations (steps 3-4), and the updating of the count register (step 5) are all performed during one iteration (see p.25-268 line 5), which is taken to be an execution phase, as its one phase of execution of the REP instruction.

14. Regarding claim 20, the *Pentium Processor Family Developer's Manual* has taught the method of claim 10, further comprising the steps of:

a. Storing data in a register file including a plurality of general purpose registers (see p.3-8),

b. Recalling data from an instruction designated general-purpose register for supplying an operand to a functional unit (see Sec.1.3.3 on p.1-7),

c. Storing destination data generated by a functional unit in an instruction designated general-purpose register (see Sec.1.3.3 on p.1-7),

d. Designating via the conditional branch-decrement instruction one of said general purpose registers as said selected test register (see "While CountReg<>0" on p.25-267). Here, the test register is CX/ECX, which is a general-purpose register, which is selected by the REP instruction. Although the REP instruction cannot specify a different register, it is still selecting the CX or ECX register to be used as the test register.

Claim Rejections - 35 USC § 103

15. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

16. Claims 11 and 21-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over the *Intel Pentium Processor Family Developer's Manual Vol.3: Architecture and Programming Manual* in further view of Hsu, U.S. Patent No. 5,901,318.

17. Regarding claim 21, the *Intel Pentium Processor Family Developer's Manual* has taught the method of claim 20 as shown above, but has not explicitly taught wherein the method further comprises:

a. Testing a predicate register selected by the conditional branch-decrement instruction to determine if the contents of the predicate register meet a second condition,

b. Designating via the conditional branch-decrement instruction one of said general purpose registers as said predicate register.

18. However, Hsu has taught instructions specifying a predicated register, which based on the value in the specified register, conditionally executes the instruction it is associated with, thereby removing conditional branches and producing more easily pipelined code (see Col.1 lines 45-52). Here, the value of the predicate register is tested at execution time to determine if the instruction is to be executed (see Col.1 liens 45-52). One of ordinary skill in the art would have recognized that easily pipelined code executes faster as fewer stalls and bubbles are present. Therefore, one

of ordinary skill in the art would have found it obvious to modify the method of the *Intel Pentium Processor Family Developer's Manual* to specify a register in an instruction to be used as a predicate register in determining whether the instruction should be executed in order to remove conditional branches and create more easily pipelined code.

19. Regarding claim 22, Hsu in view of the *Intel Pentium Processor Family Developer's Manual* has taught the method of claim 21 above, but has not explicitly taught wherein said step of designating said predicate register designates said predicate register from a predetermined subset of said general-purpose registers as said predicate register.

20. However, one of ordinary skill in the art would have recognized that the amount of bits that can be used to specify operands in an instruction word is at a premium as instructions have a fixed length, and thus one would specify only a subset of all available registers if needed to that fewer bits are needed to specify which register is being selected. Therefore, one of ordinary skill in the art would have found it obvious to modify the method of the *Intel Pentium Processor Family Developer's Manual* in view of Hsu to designate the predicate register from a predetermined subset of the general-purpose registers.

21. Claims 23 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over the *Intel Pentium Processor Family Developer's Manual Vol.3: Architecture and Programming Manual* in further view of O'Connor, U.S. Patent No. 5,8484,288.

22. Regarding claim 23, the *Intel Pentium Processor Family Developer's Manual* has taught the method of claim 10 as shown above, but has not explicitly taught wherein:

a. Said step of fetching instructions fetches a fetch packet of a predetermined plurality of instructions,

b. Said step of providing a branch address to the program counter adds a displacement value to said predetermined address boundary of said fetch packet containing said conditional branch-decrement instruction.

23. However, O'Connor has taught the fetching of a predetermined number of instructions comprising a bundle (see Col.2 lines 55-61) so that multiple instructions can be issued each clock cycle to improve code execution speed (see Col.1 lines 15-35). Therefore, one of ordinary skill in the art would have found it obvious to modify the processor of the *Intel Pentium Processor Family Developer's Manual* to fetch packets of instructions so that they can be issued in parallel, thus improving execution speed. Furthermore, Official Notice is taken that branch instructions provide an offset to the program counter when branching. Therefore, one of ordinary skill in the art would have found it obvious to modify the processor of *Intel Pentium Processor Family Developer's Manual* to provide an offset to a branch instruction fetched in a fetch packet (see above paragraph 8).

24. Regarding claim 24, *Intel Pentium Processor Family Developer's Manual* in view of O'Connor has taught the method of claim 23 above, wherein:

a. Reading a predetermined bit of each instruction to determine an execute packet of instructions capable of execution in parallel on a plurality of functional units, wherein an execute packet may include instructions in two sequential fetch packets (see O'Connor Col.2 line 63 – Col.3 line 15 and Col.4 lines 26-44),

b. Dispatching each instruction of each execute packet to a corresponding functional unit in parallel (see O'Connor Col.4 lines 1-25),

c. Said step of providing a branch address to the program counter adds said displacement value to said last predetermined address boundary of a second sequential fetch packet if said second sequential fetch packet contains said conditional branch-decrement instruction (see O'Connor Col.2 line 63 – Col.3 line 15). Here, if the end of the bundle is a conditional branch instruction, the displacement value is added and the branch instruction is executed (see above paragraph 23).

Allowable Subject Matter

25. Claims 1-2, 4 and 15-19 are allowed. The following is a statement of reasons for the indication of allowable subject matter: The applicant has stated on lines 1-12 on p.15 of the current amendment that the prior art of record has taught the modification of the test register being an unconditional operation, while the invention as claimed in claim 1 recites the decrement circuitry conditionally providing a decremented value of the test register to the test register. The examiner agrees with the applicant's argument. The prior art of record has taught a microprocessor that executes a branch-decrement instruction which provides a branch address if the contents of the test register meet a condition, and the subsequent unconditional modification of the test register, such as in "while" or "repeat-until" loop situations that update their test register contents even though the loop is known to be exiting. However, the prior art of record has not taught the combination of a microprocessor that executes a branch-decrement instruction which provides a branch address if the contents of the test register meet a condition and the

subsequent conditional modification of the test register. Therefore, the claims are allowable over the prior art of record as no combination of prior art can read upon the invention as claimed.

Conclusion

26. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

27. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Applicant is reminded that in amending in response to a rejection of claims, the patentable novelty must be clearly shown in view of the state of the art disclosed by the references cited and the objections made. Applicant must also show how the amendments avoid such references and objections. See 37 CFR § 1.111(c).

28. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Barry J. O'Brien whose telephone number is (703) 305-5864. The examiner can normally be reached on Mon.-Fri. 6:30am-4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703) 305-9712. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

29. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Barry J. O'Brien
Examiner
Art Unit 2183

BJO
3/18/2004

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